ENGG1000
Engineering Design and Innovation

Session 1, 2011

Supplementary Details for Projects in the School of Electrical Engineering and Telecommunications

Introductory Note
ENGG1000 is a single course coordinated by the Faculty of Engineering. Most of the course is run by individual schools within the Faculty, through a collection of structured projects. This document provides supplementary information which is specific to projects undertaken within the School of Electrical Engineering and Telecommunications (EE&T); it is intended to be read in conjunction with the faculty-wide course outline, which you should have received in the first lecture, but may also obtain via Moodle (http://moodle.eng.unsw.edu.au/moodle).

Course Staff within the School of EE&T
EE&T Project Coordinator: Dr Alex von Brasch
Office: EE338 Phone: 9385 4933 Email: a.vonbrasch@unsw.edu.au
Consultation times: Alex will be available during most scheduled laboratory times, and is also available for consultation in his office from 5pm to 5:45pm on Mondays and Thursdays during the semester. Due to his joint appointment in industry, Alex will generally not be in his office on other days.
Staff Mentors: Each student will be assigned to an individual mentor group, with guidance from members of academic staff. 15% of the marks are derived from your mentor’s assessment of your learning and participation.
Laboratory Demonstrators: Each laboratory will be staffed by a number of experienced demonstrators.

Course details
Credits: The course is a 6 UoC course; expected workload is 10 hours per week throughout the 13 week session.
Contact hours: The course comprises lectures and laboratory work up to 5-6 hours per week, depending on the activities scheduled in each week (refer to schedule below in this outline and also the faculty-wide schedule in the Faculty ENGG1000 Course Outline).

Lectures: EE419, starting Thursday, Week 2, 2pm. Note that there will also be some faculty-run lectures in various locations through the course.

Laboratories: Mondays 3-6pm, and Thursdays 3-6pm, in EE101/102/113/114, all on the 1st floor of the EE building.

Mentor Group Locations: Various locations – see the ElecEng project website teaching site Moodle (http://moodle.eng.unsw.edu.au/moodle) in Week 2 for more details.

Course Information

Aims within the School of EE&T

The main aims of ENGG1000 are clearly explained in the Faculty Course Outline. In keeping with these, the EE&T project aims to provide a framework for experiential learning, to introduce you to the design process, and to familiarize you with the many facets of engineering projects. Within the school, however, there are some specific additional aims:

- To convey some basic details of the principles of electrical devices, construction of electronic circuits and analysis techniques, in order to design, build and test simple circuits.
- To familiarize you with the test equipment available in the electronics laboratories, in order to evaluate your design effectively.
- To motivate the learning you will undertake in future courses, both in science and engineering, through a practical design problem.

Perhaps unlike some other projects in ENGG1000, many students may not begin the course with much experience in building circuits or measuring electrical quantities. This course provides a fairly gentle (and hopefully fun!) introduction to electronic circuits, while keeping the emphasis on engineering design.

Learning outcomes

Additionally to the faculty learning outcomes, on successful completion you should be able to:

- Appreciate some of the design challenges faced by electrical, telecommunications and photonics engineers, and what kinds of skills and knowledge are needed to tackle them.
- Give examples of design trade-offs typically experienced during electrical design.
- Explain the types of applications of simple electronic circuits, and suggest circuit designs for simple problems.
- Understand basic electrical quantities, in particular voltage and current, from a practical perspective: how to measure them and what values to expect for a given circuit design or application.

- Suggest approaches for debugging simple design problems.

**Teaching strategies**

The teaching strategies are explained in more detail in the faculty course outline. Like other projects, the teaching in the EE&T component of this course is centred around the project. For example, you will develop communication skills by communicating about the project; you will develop teamwork and project management skills in endeavouring to accomplish your project on time; you will experience the kinds of technical problems that engineers deal with on industrial projects; you will learn the importance of identifying sub-systems within a design and planning carefully for their integration by solving a complex problem; you will develop design skills by following a design process, by evaluating and comparing designs and by reflecting on them; you will learn information literacy as you sift through large amounts of information to focus in on exactly what you need to propose and implement your design. Although other courses in your degree may vary in their teaching strategy, your understanding of and ownership of the learning process developed in this course will prove invaluable for the remainder of your degree program.

The course consists of lectures, labs and tutorials. The lectures will provide the rationale for the design process followed in the course and some basic electrical engineering principles to act as a starting point for addressing the design brief. The labs and mentor meetings are intended to provide guidance on your self-directed path of discovering the relevant information and skills needed to successfully complete the project.

Mentor meetings in particular have been found to provide a very effective means of transferring knowledge and guidance. Each project team, of approximately 6 students, meets with an academic staff mentor for 1 hour in each of weeks 2 through 12. Mentors facilitate discussions of the design process and help you to reflect upon your learning in the course. Mentors will expect to see your laboratory notebooks and discuss your design ideas with you, and will expect to see teams meeting regularly, developing action points for team members, and follow-up on these by individuals. Mentors can help you to understand design concepts, background knowledge in electronic circuits, and many other things, but you need to take the initiative to use this resource by coming prepared to your mentor meetings, with questions. Mentors can also help to put the role of other classes such as Maths and Physics into perspective with respect to engineering design. Mentors will assess your individual learning and contribution to your team’s design project. Your design proposal will be marked by your own mentor, but your final report will be marked by another group’s mentor. This provides calibration data to help equalize scores given by different markers and also motivates you to write clearly for others to read your work.

**Relation to other courses**

Within the School of EE&T there are courses on design and innovation at nearly every level of the curriculum: in third year, ELEC3117 is a design course in which a
substantive project is undertaken, while in fourth year, ELEC4123 builds on students’ design proficiency and in most cases design is an aspect of the final year honours project. ENGG1000 can thus be seen as an introduction to a design theme that runs throughout electrical/telecommunications/photonics engineering.

ENGG1000 also provides introductory level knowledge of aspects of electrical energy, electronics, telecommunications and control systems, which together form the majority of courses within the EE&T degree programs.

**Assessment Specific to the EE&T Project**

Assessment in the EE&T project has similar components to the other projects throughout the faculty. The emphasis in ENGG1000 is on continual learning and continual assessment – rather than having one large assessment activity (like a final exam), you are continuously assessed throughout the semester. Success in ENGG1000 requires a student to remain actively involved, up-to-date, and work consistently throughout the semester. This is not unlike the demands on a practicing engineer in industry – good engineering is not done over-night, but through consistent hard-work and diligence, and continual planning.

<table>
<thead>
<tr>
<th>Assessment</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1 - Faculty-wide design process (individual – Week 2)</td>
<td>5%</td>
</tr>
<tr>
<td>A2 - Web Calibrated Peer Review (individual - Weeks 5, 7, 10)</td>
<td>5%</td>
</tr>
<tr>
<td>A3 - Laboratory skills test (individual)</td>
<td>10%</td>
</tr>
<tr>
<td>A4 - Circuit design principles test (individual)</td>
<td>10%</td>
</tr>
<tr>
<td>A5 - Active learning, planning and participation, assessed by mentors</td>
<td>10%</td>
</tr>
<tr>
<td>(individual: 5%, group: 5%)</td>
<td></td>
</tr>
<tr>
<td>A6 - Design notebooks, assessed by mentor and lecturer (individual)</td>
<td>5%</td>
</tr>
<tr>
<td>A7 - Lab Checkpoints (group)</td>
<td>5%</td>
</tr>
<tr>
<td>A8 - Design proposal report and presentation, marked by the mentor (group)</td>
<td>10%</td>
</tr>
<tr>
<td>A9 - Acceptance testing (group)</td>
<td>10%</td>
</tr>
<tr>
<td>A10 - Final testing (group)*</td>
<td>15%</td>
</tr>
<tr>
<td>A11 - Final design report, marked by a different mentor (group)*</td>
<td>15%</td>
</tr>
</tbody>
</table>

* This mark is moderated by peer assessment (see below)

The assessment is thus evenly distributed between individual and team marks, reflecting the requirement of the project. Experience from previous semesters shows that well-organised groups that communicate, set high standards, self-organise and resolve conflicts effectively succeed in the project.

A detailed description of each of these assessment components:

ENGG1000 Engineering Design and Innovation: Information for EE&T Project
A1 - Faculty-wide design process
This is a short essay style written assignment, based on your experience during the Impromptu Design Activity. The Impromptu Design Activity is held on Thursday of Week 1, and this assessment task takes place during the lecture time on Monday in Week 2. This assessment is run by the Learning Centre.

A2 - Web Calibrated Peer Review
The Learning Portfolio tracks your thought process during the initial design process. Three phases are assessed at different stages through the course: the Problem Definition Phase; the Conceptual Design Phase; and the Evaluation Phase. Each phase will correspond to a separate submission – denoted A2a, A2b, and A2c on the schedule. This activity consists of a short reflective essay submitted using a web-based tool called WebCPR – the link will be available through the course page on Moodle. You are then required to assess the written assignments of your peers. The aim is to develop the skills to critically assess your own work and that of your peers.

A3 - Laboratory skills test
The laboratory skills test will assess your familiarity with basic circuit construction, circuit analysis, and laboratory equipment, gained while completing the introductory labs, and will give you feedback on your understanding. Marks will be assigned by lab demonstrators according to pre-determined criteria.

A4 - Circuit design principles test
The circuit design principles test will assess your understanding of simple circuit analysis and design using a written exam of 30 min duration. Marks will be assigned based on the correctness of your answers.

A5 - Active learning, planning and participation
The learning, planning and participation mark will be assigned by your mentor. This will be based on the performance and attendance of each individual and group during the weekly mentor meetings (which are compulsory). Part of this mark also comes from the submission of a project plan in Week 4. High marks will be given for the following:
Individual: Committed to project, actively contributing to mentor meetings and non-timetabled meetings, to the design and its implementation and testing, and to the written submissions. Demonstrates commitment to the success of the group (as defined by the group at the beginning of the project) and helps the group to function effectively.
Group: Has clear goal that everyone follows. Generates, records and follows up action points from meetings (which should be held regularly outside of timetabled hours). Works well together. Is motivated. Can resolve conflicts effectively. Generates a realistic and detailed plan that everyone sticks to (revisions agreed by the group are allowed).

A6 - Design notebooks
Note taking and record taking is an important skill that is required in every engineer. Lab notebooks are a means of recording design, technical and organizational information for
later use, and are a helpful tool both during study and in professional life. Each student is required to keep a Design Journal, keeping a written record of your thoughts on the design problem, your solutions, and your work on the problem. This journal can also double as your lab book.

Design notebooks will be assessed according to the following criteria: purpose of notes (why were they made?), date (when were they made?), clarity (could someone else understand them?), detail (e.g. if you sketch your circuit diagram, could someone else build it exactly from the sketch?), completeness of experimental notes, and evidence of research or individual input (i.e. repeating lecture notes will not attract marks). Marks will be assigned in week 12, but mentor will request to view your notebook at every mentor meeting.

A7 - Lab Checkpoints

The compulsory lab program is important in this course as the primary activity in which your group will gain the required knowledge and practical experience in electronics to be able to successfully complete the project. The lab program consists of a series of exercises in which you construct a variety of useful circuits with relevance to the project. Completion of these exercises should provide the group with the background to successfully implement the design choices it makes.

As with real engineering projects it is not necessary that every individual within the group have all of the knowledge to implement the solution, but it is necessary that as whole the group has all this requisite knowledge. Hence it is required that your group completes all of these lab checkpoint before Week 8, but exactly how your group manages and allocates these checkpoints amongst group members is your choice.

A8 - Design proposal report and presentation

Written communication is consistently among the top priorities for engineering employers, and developing report writing skills are an important aspect of design and innovation. The criteria for assessing the design proposal and final design reports are given on the respective report cover sheets. The written submission is A8a.

Verbal communication is an equally important skill for every engineer. You will present your design to your mentor, as assessment A8b. This will be a short 15-20 minute verbal presentation of the group’s proposed design and plan for completion of the project. The design team should treat the mentor as a client for this task. The group will be assessed on the clarity and professionalism of the presentation, as well as the use of verbal and non-verbal cues.

A9 - Acceptance testing

Prior to taking part in the final design competition testing, the design team must demonstrate that it can meet certain basic functional requirements, as well as meeting the required safety standards. You think of this as the group being asked to demonstrate that it can meet each of the components required in a solution to the design challenge, prior to these being integrated into a fully-functional final solution. Details of Acceptance Testing will be given closer to the date.
A10 - Final testing

This will reflect the performance of your prototype in competition in Week 13. Firstly, you will be assessed on how well your prototype meets the design aims in the practical testing. This will be a two part evaluation of your prototype. The first part will be evaluated on the performance of your prototype in a competition and will constitute 70% of the mark for this task. The second part will be a subjective assessment of your prototype by a panel of judges against the criteria specified in the project brief and will constitute the remaining 30% of the mark. The details and marking criteria used during the testing are given in the EE&T project brief.

A11 - Final design report

Then you will prepare a final report on the results of prototype testing. The report will be in the form of a professional summary reflecting on what was achieved, why it worked out the way it did and how the results could have been better, construction methods and issues, lessons learned and a critique on the effectiveness of your group’s performance.

PA - Peer Assessment

The final testing and final report marks will be moderated on an individual basis by peer assessment. Peer assessment will be conducted as follows:

Peer Assessment will be conducted using a web-based tool called WebPA – this will be available as a link through Moodle. At two points throughout the session you will be asked to score all your fellow team members on their contribution to the project. The scores of your team members will be averaged to produce a peer assessment score for the project.

This score will then be used to moderate the final testing and final report marks, i.e. if you contribute little to the team, then your final testing and final report marks may be lower than for others in the team, while if you are a strong contributor to the team, then your final testing and final report marks may be higher than for others. The peer assessment will be applied as an individual weighting to the final testing and final report marks.

Peer assessment is an important part of assessing group projects, because your contribution to the team is vital to the team’s success.

Late submissions of assessed work attract a penalty of 5% per day, including weekends. After 10 days, a mark of zero will be awarded.
## Course Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Monday</th>
<th>Thursday</th>
<th>Assessment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2:00 Introductory lecture <em>(Clancy Auditorium)</em></td>
<td>2:00 <strong>Impromptu design</strong> (assessable) – see faculty outline. Venues advised at Monday Week 1 lecture or online</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2:00 <strong>Review impromptu design</strong> (assessable) – see faculty outline</td>
<td>2:00 Lecture 1 (EE419) 3-4 or 4-5: Mentor meeting 1</td>
<td>A1</td>
</tr>
<tr>
<td>3</td>
<td>2:00 Lecture 2 (EE419) 3-6: Laboratory*</td>
<td>2:00 Lecture 3 (EE419) 3-5: Mentor meeting 2 3-6: Laboratory*</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>2:00 Lecture 4 (EE419) 3-6: Laboratory*</td>
<td>2:00 Lecture 5 (EE419) 3-5: Mentor meeting 3 3-6: Laboratory*</td>
<td>A5–Project plan to mentor A2a</td>
</tr>
<tr>
<td>5</td>
<td>2:00 Lecture 6 (EE419) 3-6: Laboratory*</td>
<td>2:00 Lecture 7 (EE419) 3-5: Mentor meeting 4 3-6: Laboratory*</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>2:00 Lecture 8 (EE419) 3-6 Laboratory skills test*</td>
<td>2:00 Lecture 9 (EE419) 3-5: Mentor meeting 5 3-6: Laboratory*</td>
<td>A2b, A3</td>
</tr>
<tr>
<td>7</td>
<td>2:00 Lecture 10 (EE419) 3-6: Laboratory*</td>
<td>2:00 Circuit Principles Test (TBA) 3-5: Mentor meeting 6 3-6: Laboratory*</td>
<td>A4</td>
</tr>
<tr>
<td>8</td>
<td>2:00 Lecture 11 (EE419) 3-6: Laboratory*</td>
<td>2:00 Lecture 12 (EE419) 3-5: Mentor meeting 7 3-6: Laboratory*</td>
<td>A7, A8a</td>
</tr>
<tr>
<td></td>
<td><strong>MID-SEMESTER BREAK</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>2:00 Lecture 13 (EE419) 3-6: Laboratory*</td>
<td>2:00 Lecture 14 (EE419) 3-5: Mentor meeting 8 - Presentation</td>
<td>A2c, A8b</td>
</tr>
<tr>
<td>Week</td>
<td>Monday</td>
<td>Tuesday</td>
<td>Wednesday</td>
</tr>
<tr>
<td>------</td>
<td>--------</td>
<td>---------</td>
<td>-----------</td>
</tr>
<tr>
<td>10</td>
<td>2-5: Acceptance Testing (TBA)</td>
<td>3-6: Laboratory*</td>
<td>2:00 Lecture 15 (EE419)</td>
</tr>
<tr>
<td></td>
<td>3-6: Laboratory*</td>
<td>3-5: Mentor meeting 10</td>
<td>3-6: Laboratory*</td>
</tr>
<tr>
<td>12</td>
<td>2-6: Laboratory*</td>
<td>3-5: Mentor meeting 11</td>
<td>2-6: Laboratory*</td>
</tr>
<tr>
<td>13</td>
<td>2-5: Final Testing (TBA)</td>
<td>2-3: End of Session BBQ</td>
<td></td>
</tr>
</tbody>
</table>

*EE101, 102, 113, 114

Yellow shading denotes Faculty of Engineering activities.

The Laboratories are ‘come as you are’ – there is no formal allocation or timetable. The labs will be open and staffed at the above times and no attendance will be recorded. Note, however, the Lab Skills Test and the Lab Checkpoint requirements – it is your responsibility as adults to attend the labs as often as you need to pass the course and complete your prototype.

Note that while our lab demonstrators are excellent and experienced they are also only human. If you suddenly turn up to the Lab in week 9 needing to get ten checkpoints marked, and find that the demonstrators are too busy and can’t mark you off then this is your responsibility and you will not receive these marks. It is your responsibility to ensure that you keep up-to-date in the lab program.

Some Key dates:

**Week 1 (Friday):** By now you must have **selected your project**, by following the instructions on Moodle (http://moodle.eng.unsw.edu.au/moodle)

**Week 4 (Mentor meeting):** **Submit a project plan** to your mentor. This is not assessable, but is your first opportunity for formal feedback.

**Week 8 (Mentor meeting):** Submit one design proposal per group to your mentor. A presentation on this given in Week 9.

**Week 13 (Friday):** **Submit your team’s final report (2 copies)** to the assignment drop-box outside room EEG12. Ensure that the cover sheet has been signed by all team members and that any resources borrowed have been returned to the lecturer.
Resources

Wondering where or how to get started? Here are some suggestions, from various sources:

The recommended text book for ENGG1000:


Another good one for introductory engineering design is:


Horenstein, M. N., *Design Concepts for Engineers*, Pearson/Prentice Hall, 2006 (this is an excellent text on engineering design that is better than Voland in various respects. It is written by a large team of authors, has great examples and has a fresher, more up-to-date feel than Voland)

More specifically for electrical engineering design are:

Wilcox, A. D., *Engineering Design for Electrical Engineers*, Pearson/Prentice-Hall, 1989 (this interprets design perhaps more closely to EE&T than the others, and in various sections discusses aspects of specific relevance to Electrical Engineering)


More technical books that may help (most helpful in bold) include:

Brindley, K., *Starting Electronics*, Elsevier, Burlington, MA, 2005. (very clearly written, this is an excellent introduction to electronics for anyone new to the subject) – in UNSW library


Scherz, P., *Practical Electronics for Inventors*, McGraw-Hill, 2000 (this is a very helpful book on introductory electronics, and includes example circuits and practical design tips) – in UNSW library


Carlson, A. B., and Gisser, D. G., *Electrical Engineering: Concepts and Applications* (this is not a design text, but is written at about the right level to provide a useful resource for circuit analysis)

Also:

The EE&T project website linked through the course website (moodle.eng.unsw.edu.au) (will be updated as the semester unfolds)


Selinger, C., *Stuff you don’t learn in engineering school: Skills for success in the real world*, Wiley, 2004 (how to work in a team, etc. Read it for interest, or before you do your industrial training)


Circuit example web sites, for example:

http://www.aldinc.com/ald_circuitideas.htm
http://www.discovercircuits.com/list.htm
http://www.allaboutcircuits.com/
http://www.opencircuits.com/Basic_Circuits_and_Circuit_Building_BLOCKS
http://www.kpsec.freeuk.com/trancirc.htm
http://www.eleinmec.com/index.asp
http://hobby_elec.piclist.com/e_pic.htm (PIC microcontrollers)

**Preparation for Laboratories**

You are advised to do the following in preparation for your first electronics laboratory:

Wear covered shoes. Without these you will be refused entry to all Electrical Engineering labs.

Obtain a prototyping board before the first lab. If you do not own one, you can purchase one from the Electrical Engineering School Office for $15.

You may also find it helpful to have a small pair of pliers and a set of small screwdrivers.

Read the laboratory safety manual (http://scoff.ee.unsw.edu.au/forms/Safety_Manual_UG-Feb2009-final.pdf) and view the safety video (http://emedia.ee.unsw.edu.au/contents/ElectricalSafety.wmv) and sign the OH&S form (http://scoff.ee.unsw.edu.au/forms/Safety_Forml_UG-v08.pdf) or agree online (https://comp1.ee.unsw.edu.au/~eet/studentLogin/index.php) before the first lab. **Under no circumstances is 240V to be used at any stage during this course.**
Get a lab notebook if you don’t already have one, and bring it to every lab (and every mentor meeting and team project meeting).

Read the laboratory exercises in advance of the lab (when attempting the suggested introductory labs).

Read the related lecture notes in advance of the lab, and bring them to the lab.

If you expect to do soldering (more likely in the later labs), bring safety goggles or purchase them from the Electrical Engineering School Office for $5.

The Electronics Workshop is located in room G15, on the ground floor of the Electrical Engineering building. The staff in the Electronics Workshop are very friendly and helpful. Any of the components whose datasheets appear on the course web-site at moodle.eng.unsw.edu.au may be obtained from the Electronics Workshop free of charge, although limits may apply to the quantities you can request. You should, however, bring a component request form, signed by one of the laboratory demonstrators. This form may also be found on the course web-site.

Other Matters

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other peoples work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a serious offence by the University and severe penalties may apply. Instances of plagiarism were detected in submitted work in the ENGG1000 ElecEng project during 2009, and penalties were applied. For more information about plagiarism, please refer to http://www.lc.unsw.edu.au/plagiarism, or seek advice from course staff.

Continual Course Improvement

The course is under constant revision in order to improve the learning outcomes of its students. Many positive comments have been received about the EE&T project stream of ENGG1000 in previous years, and all successful aspects of the course have been retained. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process (surveys at the end of the course).

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School policies, see http://scoff.ee.unsw.edu.au/.
Acknowledgements

Parts of some materials for this course were developed by Prof. D. Taubman, Dr C. Reidsema, and Dr. J. Epps, all of whom have contributed greatly to the development of this course since its inception.