ELEC2141: Digital Circuit Design

COURSE INTRODUCTION – Session 1, 2011

1. Course Staff

Academic in Charge: Dr. Tara J. Hamilton  Room EE 207  t.hamilton@unsw.edu.au
Lecturer: Nonie Politi  Room EE 209  nonie@unsw.edu.au
Tutor: Nonie Politi  Room EE 209  nonie@unsw.edu.au
Laboratory Demonstrators: Gough Lui  [ GL ]  gough@unsw.edu.au
Adrian Ratter  [ AR ]  adrian.ratter@unsw.edu.au
Alan Ao  [ AA ]  p.l.ao@unsw.edu.au
Edmund Li  [ EL ]  edmund.li@student.unsw.edu.au
Chris Webb  [ CW ]  c.webb@unsw.edu.au
Sam Jiang  [ SJ ]  sam.jiang@unsw.edu.au

Consultations

There are no official consultation hours for this subject. Students may seek consultation at any convenient time in the lecturer’s office, room EE 209. Prior appointment is recommended.

Students are encouraged to post questions related to the course syllabus on the Moodle discussion forums or on the course Facebook page. Such questions will be addressed by the lecturer, other course staff and fellow students.

2. Course Details

Credits

ELEC2141 is a 6 UoC course; expected workload is 10-12 hours per week throughout the session.

Contact Hours

The course consists of 3 hours of lectures, 1 hour of tutorials and 2 hours of laboratory sessions each week.
Lectures: Tuesday 14 - 16 EE G24
and
Friday 11 - 12 EE G24

Tutorial: Tuesday 12 - 13 Quad G32
Thursday 12 - 13 Quad G44
Thursday 13 - 14 Quad G44

Laboratory: Monday 09 - 11 EE 233 GL, AA
Monday 11 - 13 EE 233 EL, AA
Monday 14 - 16 EE 233 EL, SJ
Tuesday 11 - 13 EE 233 EL, CW
Wednesday 09 - 11 EE 233 CW, SJ
Wednesday 12 - 14 EE 233 AA, CW/AR
Thursday 09 - 11 EE 233 GL, CW
Thursday 12 - 14 EE 233 GL, AR
Thursday 14 - 16 EE 233 GL, AR

Tutorial classes and the laboratory sessions start in Week 2.

3. Course Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
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<tbody>
<tr>
<td>1</td>
<td>Number Systems</td>
</tr>
<tr>
<td>2</td>
<td>Combinational Logic Circuits 1</td>
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<tr>
<td>3</td>
<td>Combinational Logic Circuits 2</td>
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<tr>
<td>4</td>
<td>Combinational Logic Design</td>
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<tr>
<td>5</td>
<td>Sequential Circuit Elements</td>
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<tr>
<td>6</td>
<td>Sequential Circuit Analysis</td>
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<tr>
<td>7</td>
<td>Sequential Circuit Design</td>
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<tr>
<td>8</td>
<td>Verilog HDL</td>
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<tr>
<td>9</td>
<td>Arithmetic Circuits</td>
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<tr>
<td>10</td>
<td>Computer Design Fundamentals</td>
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<tr>
<td>11</td>
<td>Guest Lecture</td>
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<tr>
<td>12</td>
<td>CMOS Technology</td>
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4. Resources for Students

Course Web Pages

The course web page is hosted on the Faculty of Engineering’s Moodle server, which can be accessed at: [http://moodle.eng.unsw.edu.au/](http://moodle.eng.unsw.edu.au/). All lecture, tutorial and any other notes will be available on this page, as well as access to the weekly quizzes, student marks, discussion forums and official course
announcements. It is a requirement of the course that students check this page for new announcements on a daily basis.

In addition, this course features a Facebook page, available at: [http://www.facebook.com/elec2141/](http://www.facebook.com/elec2141/). The Facebook page will share the same official course announcements as Moodle. It will also be a platform for students interaction in an informal manner and a place to get to know fellow classmates. The course staff will post articles, links and videos that, although not directly part of the course syllabus, may be of interest to the students. Students are suggested to subscribe to the page (“Like”) in order to stream new course posts directly to their news feeds.

**Prescribed Textbook**

The textbook prescribed for this course is:


Students are strongly encouraged to purchase a copy of this book as lectures will follow the book very closely and the book provides detailed explanations for most topics covered in the course. The textbook can also serve as a reference for some of the low-level material covered in ELEC2142: Embedded System Design.

**Reference Books**

The following textbooks provide alternate coverage of many of the topics discussed in lectures and constitute adequate reference material:


**5. Course Information**

**Context**

Digital systems are an integral part of many areas of engineering and technology such as personal computers, digital signal processing, telecommunications, speech analysis and recognition and control systems. The objectives of this course are to provide students with the necessary fundamental skills to design and analyze digital circuits in the real world. At the completion of the course, students should be in a position to be able to design and build reliable and cost-effective digital systems.
Aims

The course aims to provide students with fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.

6. Relation to Other Courses

The course is a second-year subject in the school of Electrical Engineering and Telecommunications at the University of New South Wales. It is a core subject for students following a BE (Electrical) or (Telecommunications) program.

Pre-requisites

The pre-requisite for this course is ELEC1111: Electrical and Telecommunications Engineering, which introduced basic concept of electrical circuits.

Following Courses

This course is a pre-requisite for ELEC2142: Embedded Systems Design, in which the digital system design concepts introduced in ELEC2141 will be applied extensively. It is also a pre-requisite for ELEC3106: Electronics, in which low-level analysis and implementation of digital devices are undertaken.

7. Learning Outcomes

The aim of this subject is to provide students with a general understanding and an appreciation of the fundamentals of digital circuits and simple microprocessor design. At the successful completion of this course, students should be able to:

- Design and analyze combinational circuits
- Display a basic understanding of standard digital circuit elements such as multiplexers, decoders, etc.
- Design and optimize simple synchronous sequential circuits
- Understand the fundamentals of the central processing unit (CPU) in a computer
- Demonstrate knowledge in practical aspects of digital circuits and systems, and their use in more complex systems
- Demonstrate understanding of the various hardware realizations of the basic digital elements
- Demonstrate basic skills in working with computer-aided design tools, including knowing the rudiments of a hardware description language (Verilog)
- Implement simple designs at various levels, from discrete components to programmable logic devices
Graduate Attributes

Graduate attributes are those which the University and the Faculty of Engineering agree students should develop during their degree. This course aims to aid students in attaining the following attributes:

- **Information literacy** – *the skills to appropriately locate, evaluate and use relevant information*, which is addressed by tutorial questions and laboratory tasks
- **The ability to engage in independent and reflective learning**, which is addressed by laboratory exercises and DVD-based learning material
- **The capacity for enterprise, initiative and creativity**, which is addressed by a design and implementation assignment
- **The capacity for analytical and critical thinking and for creative problem-solving**, which is addressed by tutorial questions, weekly quizzes and the assignment

Further information can be obtained in the document available at: [http://learningandteaching.unsw.edu.au/content/userDocs/grad_attributes.pdf](http://learningandteaching.unsw.edu.au/content/userDocs/grad_attributes.pdf).

8. Syllabus

Introduction to digital systems, number systems, binary numbers, base conversion, binary codes. Binary variables, logical operators, logic gates, Boolean functions, Boolean algebra, standard forms, two-level optimization, Karnaugh maps, don’t-care conditions, multi-level optimization, high-impedance outputs. Combinational logic design procedures, technology mapping, function blocks, multi-bit variables, encoders, decoders, multiplexers, demultiplexers. Sequential circuits, basic storage elements, latches and flip-flops structures, direct inputs, finite state machines, transition equations, state tables and diagrams, state assignments, logic diagrams, Mealy and Moore models, state minimization. Arithmetic circuits, half and full adders, cascading adders, signed numbers and 2’s complements, subtractors. Programmable devices, FPGAs, hardware description languages, Verilog implementations, simulations. Introduction to computer design, datapaths, arithmetic/logic unit (ALU), shifters, instructions set. Integrated circuits (ICs), CMOS technology, CMOS logic gates.

9. Teaching Strategies

The course consists of the following elements: lectures, tutorials, laboratory work, short quizzes and an assignment.

Lectures

The lectures form the core of this subject. Topics presented in lectures will generally be followed by detailed examples to provide students with the real-life applications. Detailed explanations of the topics will be available to students in the form of lecture notes and the prescribed textbook.
Live lectures will be video-recorded and made accessible to students for revision; however, these recordings should not be considered adequate substitutes for attending lectures in person.

**Tutorials**

The tutorial problems provide students with in-depth quantitative understanding of the topics covered in lectures. Every tutorial session will have a corresponding problem sheet that covers the topics taught in the previous week’s lectures. Students are expected to attempt the tutorial questions before attending the class and raise any problems incurred during the tutorial session.

**Laboratory work**

During the laboratory sessions, students will be introduced to real-life digital design scenarios. Each week, a new design problem related to the lectured material is presented. Students will be required to step through the problem to a complete solution using the guidelines given per lab exercise. In the first few exercises, work will be done using breadboards and discrete IC components. At a later stage, students will be taught how to use industry-standard design software and will follow similar (although simplified) design procedures used in industry. Students will need to bring their own breadboards, previously used in ELEC1111, to the laboratory. Breadboards will also be offered for sale through the school office.

A broad understanding of the tools utilized in these exercises is highly encouraged and a bonus lab task will be available to students after the successful completion of all other exercises. The bonus task will carry on from the last lab exercise and will be accompanied by minimal guidelines, allowing students to further demonstrate their ability to analyze and resolve issues independently.

**Short Quizzes**

There will be weekly quizzes throughout the semester. The purpose of the quizzes is to keep students up-to-date with the lecture material and to test basic understanding of the course concepts. Each quiz will consist of several short-answer questions that target specific topics from the previous week’s lectures.

The quizzes are delivered through Moodle and will each be made available for a period of one week between every Tuesday at 9:00am to the following Tuesday at 9:00am, after which a new quiz will become available.

**Assignment**

There will be one assignment for this subject due at the end of Week 9. The assignment will state the specifications for a desired design and will ask students to provide a verified implementation as the
result. While working towards the complete design, the students will address most of the core topics covered in lectures thus far.

Though generic guidelines will be provided, there will be no one “correct” solution to the assignment. Students will be expected to work independently, or in pairs, on their implementation and to be able to justify the unique design choices along the way.

10. Assessment

There are four components of assessment in this course:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Short quizzes</td>
<td>10%</td>
</tr>
<tr>
<td>Assignment</td>
<td>10%</td>
</tr>
<tr>
<td>Laboratory work</td>
<td>20% (+5% bonus)</td>
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<tr>
<td>Final examination</td>
<td>60%</td>
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**Short Quizzes**

The weekly quizzes will make up 10% of the overall mark. Each quiz will consist of a number of short questions and will be marked according to the number of correct answers. The quizzes are a mandatory component of the overall assessment and failure to attempt a quiz will result in no marks being given for the quiz. Each quiz will be available for a period of one week and the results per quiz will be published at the end of the period. No late attempts will be permitted. **Students must attempt at least 8 out of the 10 quizzes to pass this subject.**

**Assignment**

The assignment, which will consist of a design challenge, forms 10% of the overall mark. It will be assessed upon the successful completion of the implementation and the steps taken during the design process. Marks will be weighted towards students’ understandings and their ability to justify the design decisions. Specifications will be released at the beginning of Week 7; submissions will close at the end of Week 9. No late submissions will be accepted unless **prior approval** from the lecturer has been granted.

**Laboratory work**

The laboratory work will contribute to 20% of the overall mark. Each lab exercise will consist of number of checkpoints that will be marked by the lab assessors. Demonstrators will be available to help students with any questions or difficulties.

Upon completion of a checkpoint, students will be required to write down their student and bench numbers on the Laboratory Queue Sheet and wait for the laboratory assessor to mark their work. Students may continue working on subsequent lab tasks while waiting to be assessed. Students will be
required to show the working for each checkpoint and answer questions asked by the assessor to demonstrate their understanding of the ideas addressed within each task. Attendance to the allocated weekly lab session is mandatory and a roll will be taken at the beginning of each lab.

There are absolutely no lab exemptions given for ELEC2141. All students, including repeating ones, must complete the laboratory component for this course.

There will be 5% bonus marks available for those students who wish to attempt the additional lab task at the completion of all laboratory exercises. The bonus exercise may require a substantial amount of time to complete successfully and students attempting it are expected to work independently as there will be minimal support provided for this task.

**Final examination**

The final examination will be a 3-hour, closed-book exam dealing with material from the lectures and the supporting laboratory program. It is worth 60% of the overall mark. The questions will be in a similar style to the tutorial exercises.

**11. Other Matters**

**Academic Honesty and Plagiarism**

Plagiarism is the unacknowledged use of other peoples work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a serious offence by the University and severe penalties may apply: [http://www.lc.unsw.edu.au/plagiarism/](http://www.lc.unsw.edu.au/plagiarism/).

**Continual Course Improvement**

The course is under constant revision in order to improve the learning outcomes for students. Students are encouraged to forward any positive or negative feedback on the course to the course lecturer or the academic-in-charge.

**Administrative Matters**

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School policies: [http://scoff.ee.unsw.edu.au/](http://scoff.ee.unsw.edu.au/).