COURSE INTRODUCTION—Session 1, 2010

Course Staff
Course conveners: Dr. Aron Michael, Room EE241;
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Consultations: Consultation times through the week will be agreed upon with students in the first couple of weeks of lectures to arrive at times that suits most students. Email queries are discouraged unless it is of a very brief and trivial nature.

Course details

Credits: The course is a 6 UoC course; expected workload is about 10 hours per week throughout the 12 week session.

Contact hours: The course consist of 3 hours of lectures per week, and laboratory demonstrations will be given during lectures time when needed

Lectures: Wednesday, 6pm–9pm (EE418)

Computer Labs: Room EEG19

COURSE INFORMATION

Context and aims
This is a postgraduate course. The main focus of the subject is on semiconductor processes involved in the fabrication of very large scale silicon integrated circuits. Initially, the course will attempt to study individual processes, and towards the end these processes are integrated together into a process schedule for the fabrication of CMOS and bipolar VLSI circuits. Because integrated circuits fail
from time to time, failure analysis plays an important role in process development. The course material will include lectures on analytical techniques employed in understanding the causes of failure in order to modify the processes for better reliability.

VLSI technology is moving at a very rapid pace, spurred on by the demand for further and further miniaturisation, greater circuit complexity and functionality per chip. Minimum feature sizes in production in the ‘60s were tens of μm. In the ‘70s, it was several μm, in the ‘80s it was about 1 μm, in the ‘90s it is submicron and now in the 21stCentury, it is the deep-deep-sub micron (< 50nm range). Acronyms have evolved from SSI to MSI to LSI to VLSI to ULSI to GSI and now Terascale Integration!. The trend today is towards 3D integration. The challenges that lay ahead are enormous. In the past 20 years, ‘ultimate’ limits of scaling were predicted, only to be surpassed years later. Wafer size of 300mm is now in production and will move to 450mm by 2012!!

The subject will enable students to have a broad grasp of the multi-disciplinary nature of the VLSI technology, bringing together the know-how of physicist, chemist, engineers and mathematicians. It will provide the basics for students, who may enter the semiconductor industry, to build on. It is an exciting field of research and we should count ourselves fortunate to be witnessing and participating in this era of unparalleled ‘technology explosion’.

Aims: The course aims to ensure students become familiar with technology of silicon integrated circuits. That is, how the VLSI chip is made! Because it involves many steps, each of the step is are studied in detail and students learn how the process steps are ‘integrated’ to produce a VLSI chip.

Relation to other courses
This is a postgraduate course offered to students in the Master of Engineering Science at the University of New South Wales. The course complements the Microelectronics design courses ELEC4602 and ELEC9701. It lays the ground work for the Microsystems course ELEC9703.

Pre-requisites: Whilst there is no specific prerequisite, it is helpful for students to be familiar with semiconductor device and microelectronics design covered in EE undergraduate program under course codes ELEC4603 and ELEC4602, respectively.

Assumed knowledge: It is further assumed that the students are familiar with some basic chemistry. The course is multidisciplinary in nature.

Following courses: The course complements the Microelectronics design courses ELEC4602 and ELEC9701. It lays the ground work for the Microsystems course ELEC9703.
Old courses: The course replaces previous course code ELEC9502

Learning outcomes

After the successful completion of the course, the student will be able to:

1. Understand the basic process steps in making integrated circuits
2. Understand how these steps are integrated in the process
3. Understand the technology limitations of each process
4. Understand the impact of these limitations on the IC designer’s options
5. Develop an appreciation of the technology trends.

The course delivery methods and course content address a number of core UNSW graduate attributes; these include:
1. The capacity for analytical and critical thinking and for creative problem-solving, which is addressed by the design task and tutorial exercises.
2. The ability to engage in independent and reflective learning, which is addressed by the design task.
3. The skills of effective communication, which are addressed by the reports.
4. Information literacy, which is addressed by the homework.

Please refer to http://www.ltu.unsw.edu.au/content/userDocs/GradAttrEng.pdf for more information about graduate attributes.

Teaching strategies

This course consists of the following elements: lectures and take-home assignment work.

Lectures

The lectures, delivered in class, will cover a range of VLSI technology topics. Beginning with an overall view of the evolution in processing technology from the invention of the transistor until now. This is followed by lectures on the following topics: Si crystal growth and wafer preparation, oxidation, diffusion, implantation, epitaxy, thin film deposition, etching, lithography, metallisation, process integration and failure analysis. Emphasis is on understanding the process and its limitations; see the impact this has on process integration, the IC layout design and circuit performance.

Laboratory work

There is no formal laboratory work in this course. Some out of lecture time will be devoted, where appropriate, to visit the Semiconductor Nanofabrication Facility and see demonstration of selected processes. There will be limited exposure to TCAD simulation for some of the processes.

Home work

The lectures can only cover the course material to a certain depth; students must read the textbook and reflect on its content as preparation for the lectures to fully appreciate the course material. Students are encouraged to read the text book
and reference materials. Home preparation before attending lectures will give students maximum benefit.

**Self-guided tutorials**

The tutorials/assignments take the student through selected critical course topics, some of which may only be covered superficially, and the aim of the exercise is to make students research on the area themselves. These areas are examinable. The students are strongly encouraged to complete all the tutorial/assignments.

**Assignments:**

Two major assignments will be set for this course. Assignments will allow the student to explore the subject in greater depth. Deadline for the submission of assignment are in the course schedule.

**Assessment**

There are 2 components of the assessment in this course:

- Assignment: 30% overall weight
- Final examination: 70% overall weight
- Assessment task due dates are given in the course schedule.

**Final examination:** The exam in this course is a standard closed-book 3 hours written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Assessment is a graded mark according the correct fraction of the answers to the exam questions.

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**COURSE SCHEDULE --- ELEC9704 VLSI Technology**

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<thead>
<tr>
<th>WEEK</th>
<th>TOPIC</th>
<th>LECTURER</th>
<th>Notes</th>
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<tr>
<td>0 (29/2)</td>
<td>O-week</td>
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<tr>
<td>1(1/3)</td>
<td>Introduction VLSI technology: Review of VLSI “technology explosion” - a historical perspective of key technology advances.. Silicon crystal growth.</td>
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<tr>
<td>2(8/3)</td>
<td>Silicon crystal growth and wafer preparation</td>
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<td>3(15/3)</td>
<td>Oxidation of silicon</td>
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<td>4(22/3)</td>
<td>Impurity diffusion in silicon</td>
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<td>5(29/3)</td>
<td>Ion Implantation of impurities into silicon</td>
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<td>Date</td>
<td>Topic</td>
<td>Time</td>
<td>Assignment due</td>
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<td>6(12/4)</td>
<td>Expitaxy growth on silicon substrates</td>
<td>AM</td>
<td>Ass 1 due</td>
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<td>7(19/4)</td>
<td>Thin Film deposition techniques</td>
<td>AM</td>
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<td>8(26/4)</td>
<td>Public holiday</td>
<td>AM</td>
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<td>9(3/5)</td>
<td>Etching: wet, Reactive Plasma etching, ICP DRIE</td>
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<td>10(10/5)</td>
<td>Lithography, Metallisation</td>
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<td>11(17/5)</td>
<td>VLSI Process integration</td>
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<tr>
<td>12(24/5)</td>
<td>VLSI Process integration, 3D integration</td>
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<tr>
<td>13(31/5)</td>
<td>Failure Analysis techniques</td>
<td>AM</td>
<td>Ass 2 due</td>
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**RESOURCES FOR STUDENTS**

**Textbooks:** Prescribed textbook  
The following textbook is prescribed for the course:

JD Plummer, MD Deal, PB Griffin, “Silicon VLSI Technology”, Prentice Hall, 2000

**Reference books**  
The following books are good additional resources for topics on the course.

**Reference Books**

S K Ghandi, “VLSI Fabrication Principles”, Wiley


R A Levy, “Microelectronic Materials and Processes”, Kluwer


Books covering assumed knowledge
The following books cover material which is assumed knowledge for the course:


On-line resources
Some additional on-line resources relevant to the course:
Resource: course webct http://vista.elearning.unsw.edu.au
library resources http://info.library.unsw.edu.au/web/
services/teaching.html

CAD resources
Students will use the PCs in the CAD Laboratory (room G19 or 16) for all assignments. For specific details on how to log on, see the course web page. Students can access the CAD tools after hours on the dual boot PCs in the School computer laboratory located in room EEG19.

OTHER MATTERS

Academic Honesty and Plagiarism
Plagiarism is the unacknowledged use of other peoples work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a serious offence by the University and severe penalties may apply. For more information about plagiarism, please refer to http://www.lc.unsw.edu.au/plagiarism

Continual Course Improvement
Students are advised that the course is under constant revision in order to improve the learning outcomes of its students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process.

Administrative Matters
On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School policies, see http://scoff.ee.unsw.edu.au/. 