Integrated Nanoelectronic Circuits for Solid State Quantum Computation

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Objectives: Extraction of device capacitances for determination of charge qubit detection efficiency

Abstract & Motivation

Quantum computers

Solid state quantum computer architectures, with qubits (quantum bits) encoded using ion implanted single phosphorus atoms are now feasible given recent advances in the atomic doping of semiconductors. However, the practical implementation of a qubit is time consuming and subject to certain constraints such as misalignment in fabrication and phosphorus ion straggle. This increases the difficulty of experimental study on charge qubit and spin qubit devices.

Goal

This research is motivated to assess through modeling, the readout signal strength ($\Delta q$) as measured by an integrated single electron transistor (SET). A novel method incorporating FastCAP to extract device capacitances for determination of charge / spin qubit detection efficiency will be used to aid in the design of optimized Si:P qubit devices.

Results

4 Types of simulation:
- Ideal cases
- Extreme cases
- Monte Carlo
- 2D Maps of charge sensitivity

Prior to the results shown here, we have simulated some ideal and extreme cases to achieve consistent and accurate calculations. In Monte Carlo simulations, we obtained a mean $\Delta q$ of 0.05e for charge qubit devices and 0.437e for spin qubit devices. The result for the charge qubit device is comparable to the experimental readout (0.012e) normalized to the voltage required to transfer a single electron onto the SET island ($V$) is $\Delta q$.

Conclusion

A novel technique has been developed to assess the readout signal strength ($\Delta q$) as measured by an SET in qubit devices. The results obtained are used to aid in the design of optimized Si:P qubit devices. However, comparison with experimental results is an issue due to limited statistics of fabricated device measurements.

Future Work

Fabrication of spin qubit devices to collect more data and correlate them with the modeling results achieved here.

A paper titled “FastCAP Modeling of Si:P Qubit Devices for Solid State Quantum Computation” based on this research is in preparation to Nanotechnology.

References: